Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS

1. (Currently Amended) A processor comprising:

a bidirectional interface comprising a first interface node to output a first signal and a second interface node to receive an external signal when a dual pin mode is enabled;

output logic to assert [[a]] said first signal indicating an internal high temperature on said bidirectional interface;

throttling logic coupled to said bidirectional interface, said throttling logic to throttle operations of said processor if either said internal high temperature is indicated by said first signal or if an external signal is received on said bidirectional interface.

2. (Original) The processor of claim 1 wherein said bidirectional interface is a single interface node.

3. (Original) The processor of claim 1 further comprising:

a first path for said first signal;

a second path for said external signal;

selection logic to select between said first path which disregards the external signal in a unidirectional mode and said second path which considers said external signal in a bidirectional single interface mode.

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4. (Original) The processor of claim 3 wherein said bidirectional interface comprises a first interface node and a second interface node, the second interface node being an input, the selection logic to further select a third path in a bidirectional dual interface mode.

5. (Original) The processor of claim 4 wherein said third path comprises:

an internal signal path for said first signal having a first delay;

an external signal path for said external signal having a second delay, said first delay to match the second delay plus an external delay.

6. (Currently Amended) The processor of claim 1 wherein said bidirectional interface further comprises:

~~a first interface node to output said first signal and a second interface node to receive an external signal when a dual pin mode is enabled;~~

a single bidirectional interface node when a bidirectional mode is enabled.

7. (Original) The processor of claim 6 further comprising:

a first delay in a first path of said first signal;

a second delay in a second path of said external signal, wherein said first delay in said first path matches said second delay in said second path plus an external delay.

8. (Currently Amended) A system comprising:

a first processor comprising:

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a bidirectional interface comprising a first interface node to output a first signal and a second interface node to receive an external signal when a dual pin mode is enabled ~~a first interface node to output an internal signal indicating a high temperature~~;

~~a second interface node to receive an external signal;~~

throttling logic to throttle said first processor in response to the internal signal or the external signal;

system logic to assert said external signal.

9. (Original) The system of claim 8 further comprising:

a second processor comprising:

a second processor first interface node to output a second processor internal signal indicating a second processor high temperature;

a second processor second interface node to receive a second external signal;

second processor throttling logic to throttle said second processor in response to the second processor internal signal or the second external signal;

wherein said system logic is to assert said external signal to said first processor in response said second processor outputting said second processor internal signal indicating said second processor high temperature.

10. (Original) The system of claim 9 wherein said first processor further comprises:

a first delay in a first path of said internal signal to said throttling logic;

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a second delay in a second path of said external signal to said throttling logic, said first delay to match said second delay plus a system logic delay.

11. (Original) The system of claim 10 wherein said first processor and said second processor are to commence throttling in synchronization in response to said second processor internal signal.

12. (Original) The system of claim 11 wherein said first processor and said second processor are to commence throttling in a same single clock cycle.

13. (Currently Amended) A method comprising:

driving a first signal indicating an internally measured high temperature on a bidirectional interface comprising a first interface node to output said first signal and a second interface node to receive an external signal when a dual pin mode is enabled;

throttling operations if either said first signal is driven or if an external signal is received on said bidirectional interface.

14. (Original) The method of claim 13 wherein driving comprises:

testing if a selected thermal metric is reached;

driving the first signal if said selected thermal metric is reached.

15. (Original) The method of claim 13 wherein said interface node is a single bidirectional interface node.

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16. (Original) The method of claim 13 further comprising delaying the first signal and the external signal through different delay paths.

17. (Original) The method of claim 13 further comprising selecting either a first mode using a single bidirectional interface node as the interface node or a second mode using two interface nodes.

18. (Original) The method of claim 17 further comprising:

delaying, in the second mode, the first signal to cause throttling at the same time as another processor.

19. (Currently Amended) A method comprising:

indicating an internally measured high temperature of a first processor across a bidirectional interface comprising a first interface node to output a first signal and a second interface node to receive an external signal when a dual pin mode is enabled;

synchronizing throttling in response to the internally measured high temperature of the first processor with throttling of a second processor.

20. Canceled

21. (Currently Amended) The method of claim ~~20~~ 19 wherein synchronizing comprises:

receiving said first signal and asserting a second signal to the second processor;

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delaying at least said first processor from starting to throttle operations to allow said first processor and said second processor to throttle operations in a synchronized manner.

22. (Original) The method of claim 21 wherein delaying comprises preventing the first processor from throttling until the same clock cycle in which the second processor begins throttling.

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